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| EXAMINER |
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ALROBAYE, IDRIS N

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| ART UNIT | PAPER NUMBER |
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2183

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09/08/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

1. This action is responsive to communications through the applicant's application filed on 5/12/2008.
2. Claims 2-21 remained for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2-21 are rejected under 35 U.S.C. 102 (b) as being anticipated by Hesson et al. U.S. Patent No. 5,666,506 (hereinafter Hesson).

5. As to claim 2, 12, Hesson taught at least:

A pipelined microprocessor (see pipeline processor in col. 1, lines 29-34 for background) capable of detecting an instruction that loads data from a first memory location that was previously stored to (see comparison of instruction in col. 4, lines 64-67, col. 5, lines 1-13).

6. Hesson did not explicitly show the instruction is detected without requiring computation of an external memory address as claimed. However, Hesson taught comparison of the virtual address (see col.4, lines 65-67). Examiner holds that virtual

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address is not external, and the comparison is not computation. Therefore, Hesson is without address computation.

7. As to Claims 3, 13, Hesson taught detecting an instruction that stores data into a second memory location that was previously read from without computing an external memory address of said second memory location (see store address being compared to all load addresses in col.6, lines 35-41).

8. As to claims 4, 14, Hesson was also applicable for detecting instructions that load data from identical memory locations that were previously stored to (see col.6, lines 35-42). As to the feature of without computing external memory addresses, see discussions in Paragraph 4 above.

9. As to claims 5, 15, Hesson also taught detecting instructions that store data into identical memory locations that were previously read from (see the load were allowed to proceed after store violation in col.6, lines 13-15).

10. As to claims 6, 7, 16, 17, Hesson's virtual addresses were symbolic structure (see virtual address in col.4, lines 64-67).

11. As to claim 8, 9, 18, 19, examiner holds that virtual same address must have identical base and identical offset.

12. As to claim 10, 11, Hesson also taught a bypass element [violation condition] capable of sending a bypass signal to an instruction execution stage of pipelined microprocessor that indicates that instructions referred to an identical memory location (see store violation condition detected in co1.6, lines 35-42).

13. As to claims 20, Hesson also taught at least

- a) detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax (see virtual address comparison) for computing an effective address for the first memory location and the operands needed to compute the effective address in (see the store instruction for the first instruction in store barrier hit detection in co1.5, lines 3-13, see the virtual addresses as the syntax);
- b) detecting a second instruction that loads data from a second memory location, the second instruction comprising syntax for computing an effective address for said second memory location (see the snoop of the load instruction as the second instruction in col.6, lines 13-21).

14. Hesson did not explicitly show the determination of syntax relationship between the first memory location and said second memory location, without computing the effective address for said first memory location and without computing the effective address for the second memory location as claimed. However, Hesson, in the same patent, taught already comparison of virtual addresses of the load instruction and store

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instruction conflicts (see co1.4, lines 5667, co1.5, lines 1-13). Examiner holds that virtual address comparison is not computation. Therefore, Hesson is without address computation.

15. As to the detection of the instructions, examiner holds that for the purpose of detecting the load/store conflicts, Hesson must detect the op code of an instruction to see whether it was a load or store instruction, and virtual addresses by the instructions must comprise a syntax for computing effective address of memory location.

16. As to claim 21, Hesson was also directed to identical memory location (see the address conflicts in col.6, lines 3-29).

Response to Arguments

17. Applicant's arguments filed 5/12/2008 have been fully considered but they are not persuasive.

18. Appellant's Argument:

In addition, Applicant respectfully disagrees with the assertion by the Examiner that the virtual address operations of Hesson are "comparison" and "not computation". Applicant notes that Hesson explicitly requires a computation during the comparison. Hesson uses this computation to generate an output. The output is discussed in the remainder of the paragraph cited by the examiner.

If a store barrier cache hit results from the next instruction prefetch buffer virtual address, then the store barrier cache hit control output is a logic one. If no match is found, then the store barrier cache hit control output is a logic zero. (Col. 5, 11.9-14, Hesson)

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Since Hesson is generating an output, it is performing a computation to create that output. Therefore, Hesson does not anticipate the claimed limitation of detecting an instruction "without requiring computation of an external memory address of said first memory location for the instruction".

Examiner's Response:

The examiner respectfully disagrees with the appellant's assertion for a number of reasons. First, the examiner would like to remind the applicant's that the rejection is based on the broadest reasonable interpretation of the claim language along with explicit and unambiguous definitions for the claim language which must be made available in the specification. The instant application clearly fails to provide any definition for the term "computation". The specification appears to indicate that "computation" involves calculating the effective address based on the base value and offset value. Hesson does not show computation, it shows comparison wherein the result is either 1 or 0 (or true or false). A computation output involves more than two known values (1 or 0), it's usually arithmetic calculation. Therefore, because the applicant did not explicitly define the term 'computation' in either specification or the claims, it's understood by the examiner as arithmetic calculation which does not include comparison.

The applicant is also reminded that what is claimed is not "*without requiring computation*" per se, but "without requiring computation of an external memory address" and because Hesson is comparing virtual addresses, it has not computed an external memory address at the time it is performing the comparison.

Furthermore, applicant's specification page 8, line 20 to page 9, line 11 indicates that the load-store bypass element 121 involves examining the instructions. It implies that examining the instruction involves comparison, wherein based on the examination of the instructions, the load-store bypass generates a bypass output. The appellant argues that because Hesson generates an output, "*it is performing a computation to create the output*". According to the appellant's assertion, the instant application performs computation in order for the load-store bypass to create an output and thus contradicts applicant's claimed feature "*without requiring computation*".

Also, the examiner disagrees with the appellant's argument because the virtual address as shown by Hesson is not an external address and thus reads on the claimed limitation "*without requiring computation of an **external memory address***".

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Ameson et al. (5,475,823) is cited for the teaching of detection circuit [520] detecting the load instruction accessing a location previously stored (see fig.5, 4, lines 55-67, co1.8, lines 10-24, lines 37-48);

b) Kiyohara et al. (5,694,577) is cited for the teaching of comparison of virtual addresses of preload instructions and store instructions (see co1.2, lines 55-65, co1.5, lines 49-61);

c) Ball (5,615,357) is cited for disclosure of a system including a determination of syntax relationship (see the model of CPU) without itself calculating effective addresses of the first a and second instructions (see the trace file containing the load and store instruction effective addresses in co1.2, lines 39-45, lines 64-67, col.3, lines 1-6, co1.4, lines 1-11, co1.11, lines 59-67, see co1.10, lines 10-52 for the trace driven mode, see co1.12, lines 1-7 for load and store).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRIS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard Ellis/
Primary Examiner, Art Unit 2183

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